APPENDIX I 1.131 DECLARATION

freescale semiconductor

eIntelligence - Innovation Disclosure

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ID:	**SC11244ZC (10428)**
Title:	**M3: Motorola MisMatch Calculator**
Innovators:	Cyndi RECKER, Patrick DRENNAN
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Role	Name	Action
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m3descrip.pdf Unspecified 7.9 Kb

Name of Innovation or Engineering Development?
M3: Motorola MisMatch Calculator

What is the problem(s) to be resolved by or need(s) for your idea?
Mismatch (or matching) is a classic problem in analog circuit design. Most analog circuit blocks leverage the differential performance of devices that are in close proximity on the same chip to obtain high performance circuitry. The differential performance is mismatch. Mismatch directly affects the parametric yield loss of analog parts, and for some analog circuits, the mismatch directly determines the critical circuit performance such as bit resolution on high speed data converters.

The innovation presented here is a web-based mismatch calculator tool that allows the designer to input bias and geometry conditions for the matched pair and reports the input and output mismatch where appropriate. See attachment

Is your idea known or has it been disclosed outside of Motorola without a duty of confidence (e.g., non-disclosure agreement, joint development agreement, etc.)?
NO

Has a product incorporating your idea been sold, offered for sale, placed in production, qualification, sampled, described in any publication (including Motorola promotional literature), marketed, shipped to anyone outside of Motorola (customer or distributor), or placed into inventory?
YES, on

What is the earliest verifiable date that you communicated your idea to an individual that is NOT an innovator (e.g., the date a non-innovator witness signed your engineering notebook)?

Was your idea created or developed through work performed with a consortium, alliance, government contract, university, or joint venture?
NO

Please specify the Export Control Classification Number(s) (ECCN) to which this disclosure pertains
Unknown

None Selected

None Selected

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M3: Motorola Mismatch Calculator Description

Mismatch (or matching) is a classic problem in analog circuit design. Most analog circuit blocks leverage the differential performance of devices that are in close proximity on the same chip to obtain high performance circuitry. The differential performance is mismatch. Mismatch directly affects the parametric yield loss of analog parts, and for some analog circuits, the mismatch directly determines the critical circuit performance such as bit resolution on high speed data converters.

The innovation presented here is a web-based mismatch calculator tool that allows the designer to input bias and geometry conditions for the matched pair and reports the input and output mismatch where appropriate.

For MOSFETs and BJTs, three procedures are available. The Voltage Driven procedure allows the user to input the nodal voltages of the devices in the matched pair and reports Id (output) mismatch and Vgs (input) mismatch. The Current Mirror procedure allows the user to input the reference current and Vd on the output device and reports Id mismatch in two scenarios, with and without output conductance on the output device. The Differential Pair procedure allows the user to input the reference current and nominal Vd and reports Id mismatch and the Vgs mismatch.

The reporting of Vgs mismatch as a description of the input offset voltage is unique and innovative. Standard industry practice is to use Vt mismatch for the input offset voltage. Vgs mismatch is more accurate because it describes the dependence of the input offset voltage on bias and geometry conditions.

Results are displayed in tabular form. Included in the output table are the mismatch contributions from fundamental process and geometry parameters. This is a unique capability only available with the Motorola mismatch model and calculator. Not only does this provide mismatch process diagnostics for the technology developer but it also helps the designer better understand the mismatch problem and guides him/her to regions of better opportunity. We plan to add a feature to the software procedure that will allow the user to display the random components, the gradient components and the device sensitivities for each of the process and geometry parameters.

This tool allows for current driven and voltage driven mismatch simulations. For mismatch prediction, the bias and geometry conditions must be considered simultaneously. For example, on a MOSFET current mirror, the nominal gate voltage is dependent upon the geometry. This tool takes this in account, prior art does not.

This tool can accomodate dissimilar geometries by evaluating the mismatch contribution from both devices in the matched pair. Other tools assume the devices in the matched pair are identical. In this case, only one device in the matched pair is varied, assuming twice the variability on one device. This approach is faulty if the devices in the matched pair are not designed identically.

This tool can simulate mismatch for multiple devices in parallel and/or multiple devices in series. Other tools assume a simple pair of devices.

This tool can simulate the mismatch contributions from multiple device types in single circuit block. For example, an emitter degenerate pair contains both resistors and BJT pairs. The matching of both pairs needs to be considered simultaneously.

This tool allows for multiple bias conditions for a constant geometry. This is critical since the mismatch can vary considerable over the bias conditions which is typical of many matched circuits. Other approaches use single point solutions.